

[INCH-POUND]
MIL-M-38510/505A
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SUPERSUPNTNG
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30 August 1984

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, BIPOLAR PROGRAMMABLE LOGIC,
MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, bipolar, programmable logic microcircuits which employ titanium tungsten resistors as the fusible link or programming element. Two product assurance classes (B and S) and a choice of case outlines and lead finishes are provided and are reflected in the complete Part or Identifying Number (PIN).

1.2 PIN. The PIN shall be in accordance with MIL-M-38510 (see 3.6 herein).

1.2.1 Device type(s). The device type(s) shall be as follows:

<u>Device type</u>	<u>Circuit</u>
01	20-input 8-output AND-OR invert gate array
02	20-input 8-output registered AND-OR gate array
03	20-input 6-output registered AND-OR gate array
04	20-input 4-output registered AND-OR gate array

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Laboratory RL\ERSS, 525 Brooks Rd Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A
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FSC 5962

1.3 Absolute maximum ratings.

Supply voltage range - - - - -	-0.5 V dc to +12.0 V dc
Input voltage range- - - - -	-1.5 V dc to +12.0 V dc
Storage temperature range- - - - -	-65°C to +150°C
Lead temperature (soldering, 10 seconds) - - - -	+260°C
Thermal resistance, junction-to-case (Θ_{JC}) - -1/	(see MIL-STD-1835)
Output voltage applied - - - - -	-1.5 V dc to +12.0 V dc
Output sink current- - - - -	100 mA
Maximum power dissipation (P_D) 2/- - - - -	1.2 W
Maximum junction temperature (T_J)- - - - -	+175°C

1.4 Recommended operating conditions.

Supply voltage - - - - -	4.5 minimum to 5.5 V dc maximum
Minimum high level input voltage - - - - -	2.0 V dc
Maximum low-level input voltage- - - - -	0.8 V dc
Case operating temperature range (T_C)- - - -	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications and standards. The following specifications and standards form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
 MIL-STD-1835 - Microcircuit Case Outlines.

(Copies of specifications, standards, handbooks, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510 and as specified herein. When manufacturer-programmed devices are delivered to the user, an altered item drawing shall be prepared by the contracting activity to specify the required program configuration.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

1/ Heat sinking is recommended to reduce the junction temperature.

2/ Must withstand the added P_D due to short circuit; e.g., I_{OS} test.

3.2.2 Truth tables.

3.2.2.1 Unprogrammed devices. The truth tables for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C (see 4.4), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of fuses shall be programmed or at least 25 percent of the total number of fuses to any altered item drawing.

3.2.2.2 Programmed devices. The truth table for programmed devices shall be as specified by the altered item drawing.

3.2.3 Logic diagrams. The logic diagrams for unprogrammed devices shall be as specified on figure 3.

3.2.4 Case outline(s). The case outline(s) shall be as specified in 1.2.3.

3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510 (see 6.4).

3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I, and apply over the full recommended case temperature range.

3.5 Electrical test requirements. Electrical test requirements shall be as specified in table II and (where applicable), the altered item drawing for the applicable device type and device class. The subgroups of table III which constitute the minimum electrical test requirements for screening, qualification, and quality conformance, by device class, are specified in table II.

3.6 Marking. Marking shall be in accordance with MIL-M-38510. For programmed devices, the altered item drawing number shall be added to the marking by the programming activity.

3.7 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.7.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.2.1, tables II. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.7.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 14 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007 of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification, and quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test (method 1015 of MIL-STD-883). Test condition D using the circuit shown on figure 5, or equivalent.
- b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Parameter	Symbol	Test condition 1/ $-55^\circ \leq T_C \leq +125^\circ$ $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$	Device type	Limits		Unit
				Min	Max	
Input clamp voltage	V_{IC}	$V_{CC} = 4.5 \text{ V}, I_I = -18 \text{ mA}$	ALL		-1.5	V
High level output voltage	V_{OH}	$V_{CC} = 4.5 \text{ V}, V_{IL} = 0.0 \text{ V}$ $V_{IH} = 3.0 \text{ V}, I_{OH} = -2 \text{ mA}$	ALL	2.4		V
Low level output voltage	V_{OL}	$V_{CC} = 4.5 \text{ V}, V_{IL} = 0.0 \text{ V}$ $V_{IH} = 3.0 \text{ V}, I_{OL} = 12 \text{ mA}$	ALL		0.5	V
High level input voltage	V_{IH}	$V_{CC} = 5.5 \text{ V}$	ALL	2.0		V
Low level input voltage	V_{IL}	$V_{CC} = 5.5 \text{ V}$	ALL		0.8	V
High level input current	I_{IH}	$V_{CC} = 5.5 \text{ V}, V_I = 2.4 \text{ V}$ 2/	ALL		25	μA
Low level input current	I_{IL}	$V_{CC} = 5.5 \text{ V}, V_I = 0.4 \text{ V}$ 2/	ALL		-0.25	mA
Output short circuit current	I_{OS}	$V_{CC} = 5.5 \text{ V}, V_O = 0 \text{ V}$ 3/	ALL	-30	-250	mA
Input current	I_I	$V_{CC} = 5.5 \text{ V}, V_I = 5.5 \text{ V}$	ALL		1.0	mA
Off-state output current	I_{OZL}	$V_{CC} = 5.5 \text{ V}, V_{IL} = 0.0 \text{ V}$ $V_{IH} = 3.0 \text{ V}, V_O = 0.4 \text{ V}$ 2/	ALL		-100	μA
Off-state output current	I_{OZH}	$V_{CC} = 5.5 \text{ V}, V_{IL} = 0.0 \text{ V}$ $V_{IH} = 3.0 \text{ V}, V_O = 2.4 \text{ V}$ 2/	ALL		100	μA
Supply current	I_{CC}	$V_{CC} = 5.5 \text{ V}$	01,02, 03,04		210	mA
Propagation delay data input to output	t_{PHL}	See figure 4 4/ $C_L = 45 \text{ pF}$ minimum	01,03, 04		30	ns
Propagation delay data input to output	t_{PLH}		01,03, 04		30	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Test condition 1/ $-55^\circ \leq T_C \leq +125^\circ$ $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$	Device type	Limits		Unit
				Min	Max	
Propagation delay high impedance to output high	t_{PZH}	See figure 4 4/ $C_L = 45 \text{ pF}$ minimum	01,03, 04		30	ns
Propagation delay high impedance to output low	t_{PZL}		01,03, 04		30	ns
Propagation delay output high to high impedance	t_{PHZ}		01,03, 04		30	ns
Propagation delay output low to high impedance	t_{PLZ}		01,03, 04		30	ns
Propagation delay high impedance to output high (pin 13 to output enable)	t_{PZH}	See figure 4 5/ $C_L = 45 \text{ pF}$ minimum	02,03, 04		25	ns
Propagation delay high impedance to output low (pin 13 to output enable)	t_{PZL}		02,03, 04		25	ns
Propagation delay output high to high impedance (pin 13 to output disable)	t_{PHZ}		02,03, 04		25	ns
Propagation delay output low to high impedance (pin 13 to output disable)	t_{PLZ}		02,03, 04		25	ns
Clock to output	t_{PCH} t_{PCL}		02,03, 04		20	ns
Minimum clock pulse width	$t_{P(CL)}$		02,03, 04	20		ns
Minimum setup time	t_{SU}		02,03, 04	30		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Test condition 1/ -55° ≤ T _f ≤ +125° 4.5 V ≤ V _{CC} ≤ 5.5 V	Device type	Limits		Unit
				Min	Max	
Minimum hold time	t _H	See figure 4 5/ C _L = 45 pF minimum	ALL	0		ns
Maximum clock frequency	f _{MAX}			02,03, 04	20	MHz

- 1/ All voltages referenced to ground.
 2/ I/O terminal leakage is the worst case of I_{IX} or I_{OZX}.
 3/ Only one output shorted at a time.
 4/ Applies to nonregistered outputs only, with internal output enables.
 5/ Applies to registered outputs only, with external output enables (pin 13).

TABLE II. Electrical test requirements. 1/2/3/4/

MIL-STD-883 test requirements	Subgroups (per table III)	
	Class S devices	Class B devices
Interim electrical parameters (pre burn-in) (method 5004)	1	1
Final electrical test parameters (method 5004) for unprogrammed devices	1*, 2, 3, 7*, 8	1*, 2, 3, 7*
Final electrical test parameters (method 5004) for programmed devices	1*, 2, 3, 7*, 8, 9, 10, 11	1*, 2, 3, 7*, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group B test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11	N/A
Group C end-point electrical parameters (method 5005)	N/A	1, 2, 3, 7, 8
Group D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8	1, 2, 3, 7, 8

- 1/ (*) indicates PDA applies to subgroups 1 and 7 (see 4.2c).
 2/ Any or all subgroups may be combined when using high-speed testers.
 3/ Subgroup 7 and 8 shall consist of verifying the pattern specified.
 4/ Subgroup 8 requirements are for programmed devices only.

- c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.
- d. All devices processed by the manufacturer to an altered item drawing shall be programmed prior to burn-in.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Qualification data for subgroups 7, 8, 9, 10, and 11 shall be by attributes only.

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies the PAL device with the worst case metal mask which is processed (e.g., same mask sets excluding metal mask) and manufactured on the same certified line to the other PAL device types on this specification, then the other PAL device types may be part I qualified by conducting only group A electrical tests and any electricals specified as additional group C subgroups and submitting data in accordance with MIL-M-38510, appendix D (i.e., groups B, C, and D tests are not required for qualification).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For unprogrammed devices, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.2.1). If more than 2 devices fail to program, the lot shall be rejected. At the manufacturers option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable.
- d. For unprogrammed devices, 10 devices from the programmability sample shall be submitted to the requirements of the specified tests of subgroups 1, 2, and 3 designated for programmed devices only. If any device fails, the lot shall be rejected. At the manufacturers option the sample may be increased to 20 total devices with no more than 2 total devices failing.
- e. For unprogrammed devices, 10 devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than 2 total devices fail, the lot shall be rejected. At the manufacturers option the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883.

- a. Class S devices selected for testing in subgroup 5 (table IIa of method 5005 of MIL-STD-883) shall be programmed in accordance with 3.2.2.
- b. Electrical parameters shall be as specified in table II herein.
- c. Steady state life test for class S devices shall be in accordance with table IIa (subgroup 5) of method 5005 of MIL-STD-883 using a circuit submitted to the qualifying activity for approval. If the alternate burn-in conditions are used, the circuit on figure 4, or equivalent, shall be used.

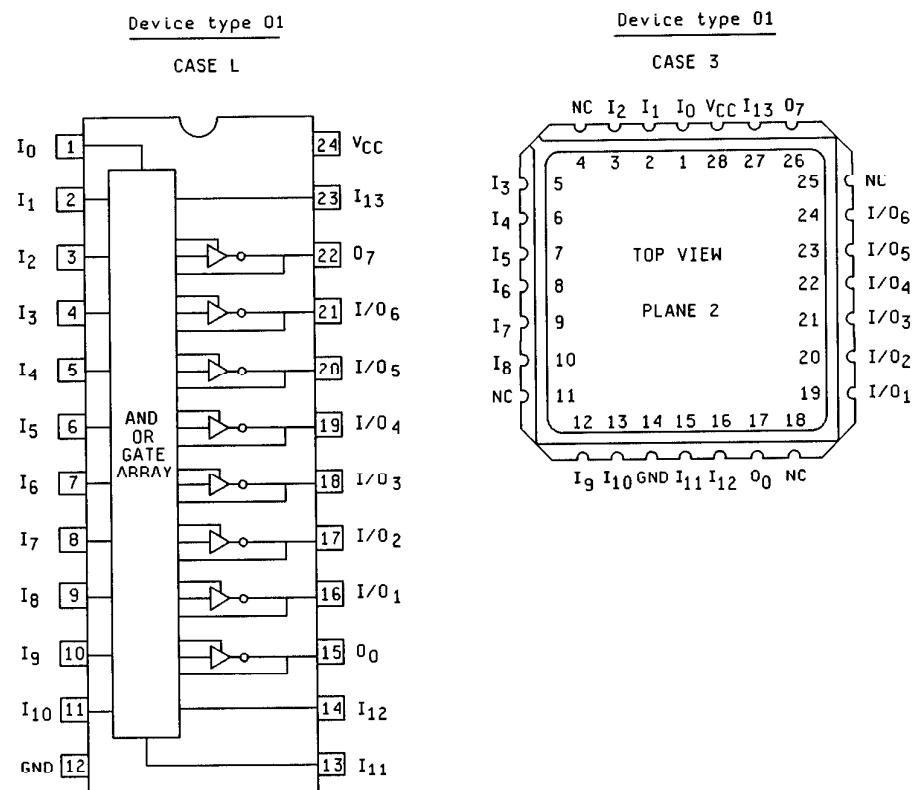


FIGURE 1. Terminal connections.

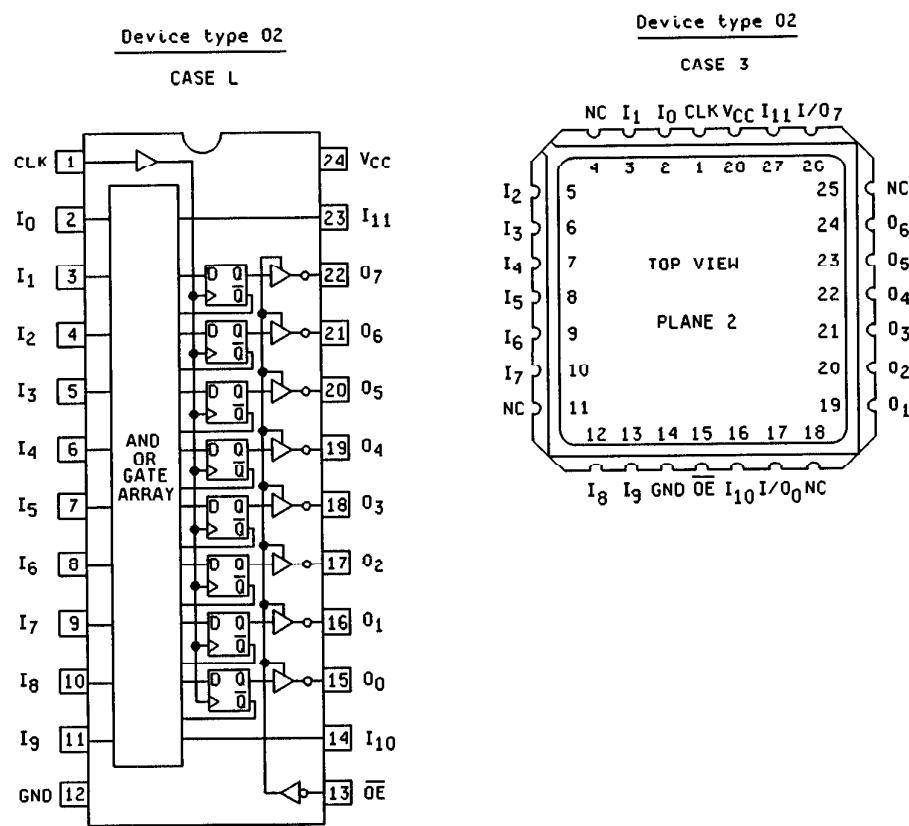


FIGURE 1. Terminal connections - Continued.

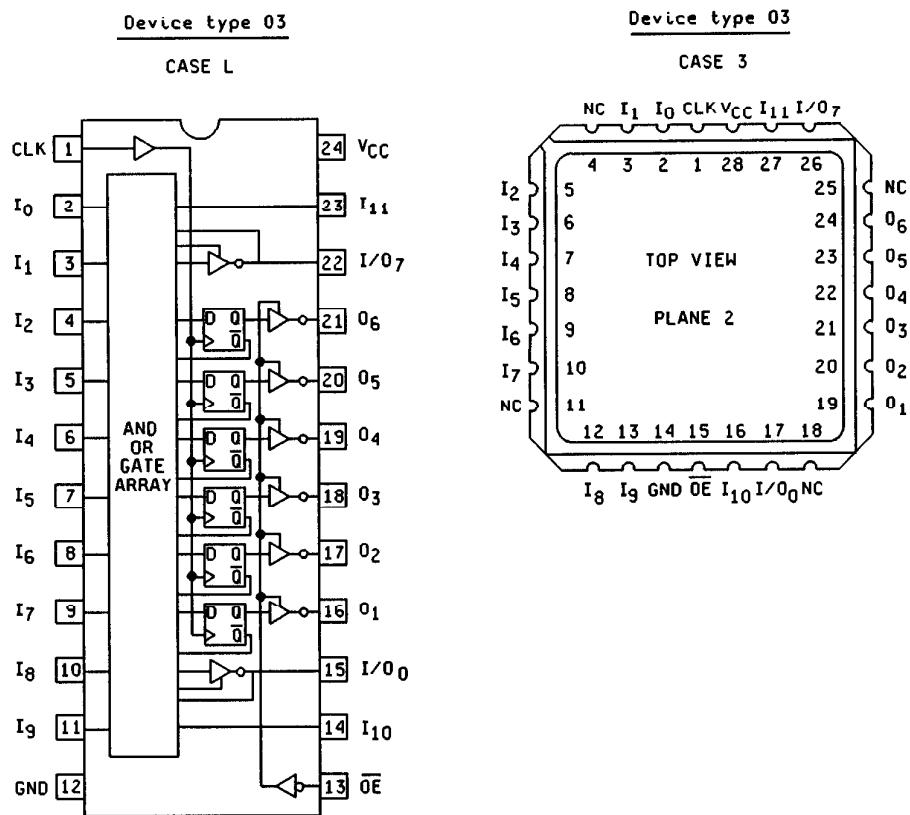


FIGURE 1. Terminal connections - Continued.

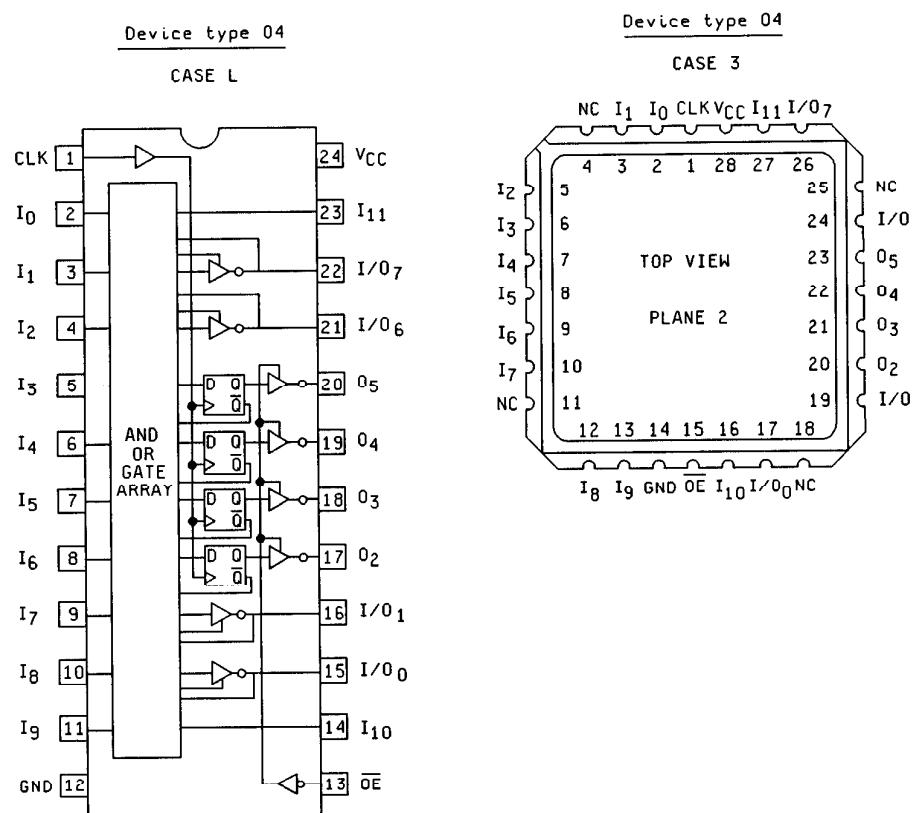


FIGURE 1. Terminal connections - Continued.

Device type 01

INPUTS															OUTPUTS							
I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0	O7	I/06	I/05	I/04	I/03	I/02	I/01	00	
X	X	X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	

Device type 02

INPUTS															OUTPUTS							
\overline{OE}	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0	CLK	O7	06	05	04	03	02	01	00	
H	X	X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	
L	X	X	X	X	X	X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	

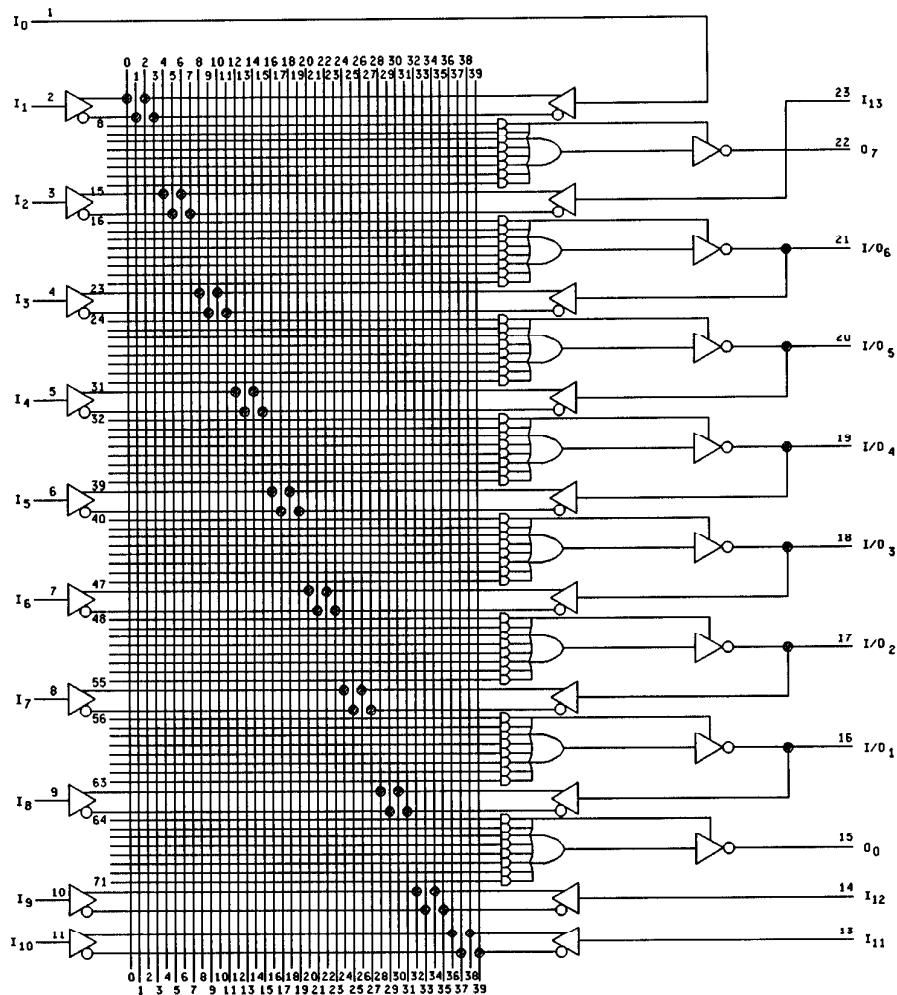
Device type 03

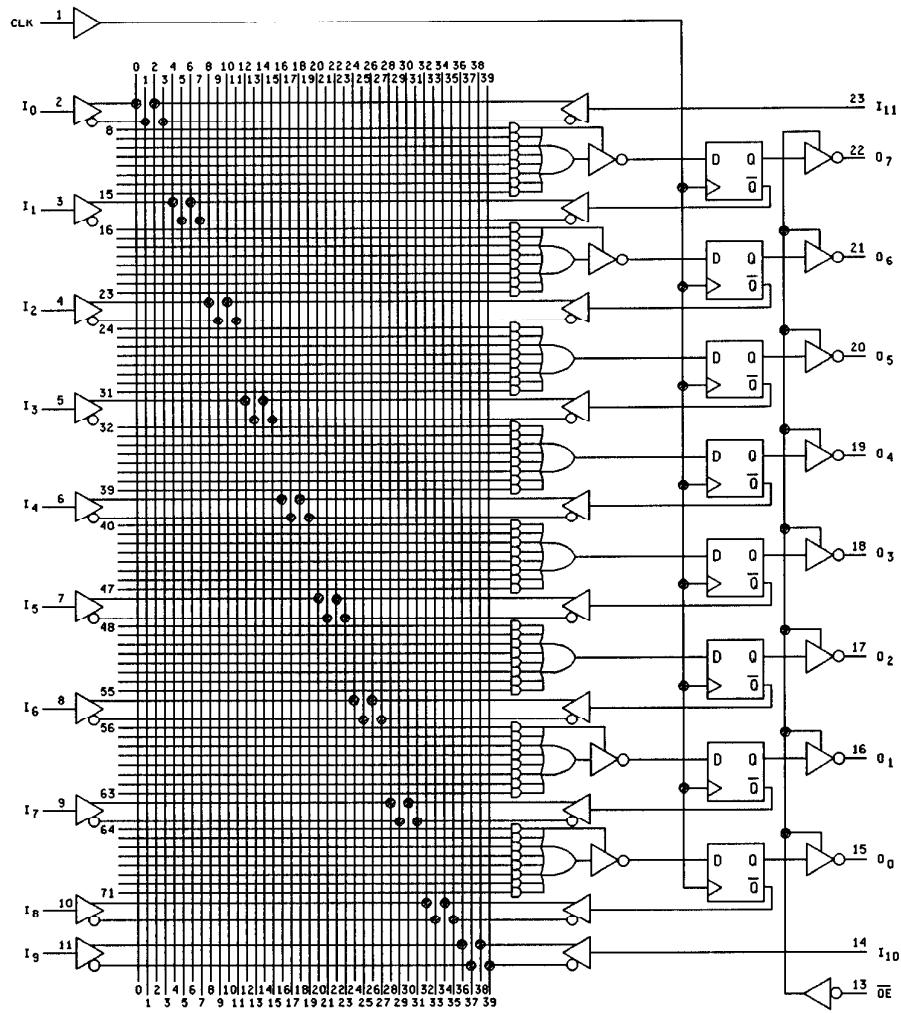
INPUTS															OUTPUTS							
\overline{OE}	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0	CLK	I/07	06	05	04	03	02	01	I/00	
H	X	X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	
L	X	X	X	X	X	X	X	X	X	X	X	X	X	Z	H	H	H	H	H	H	Z	

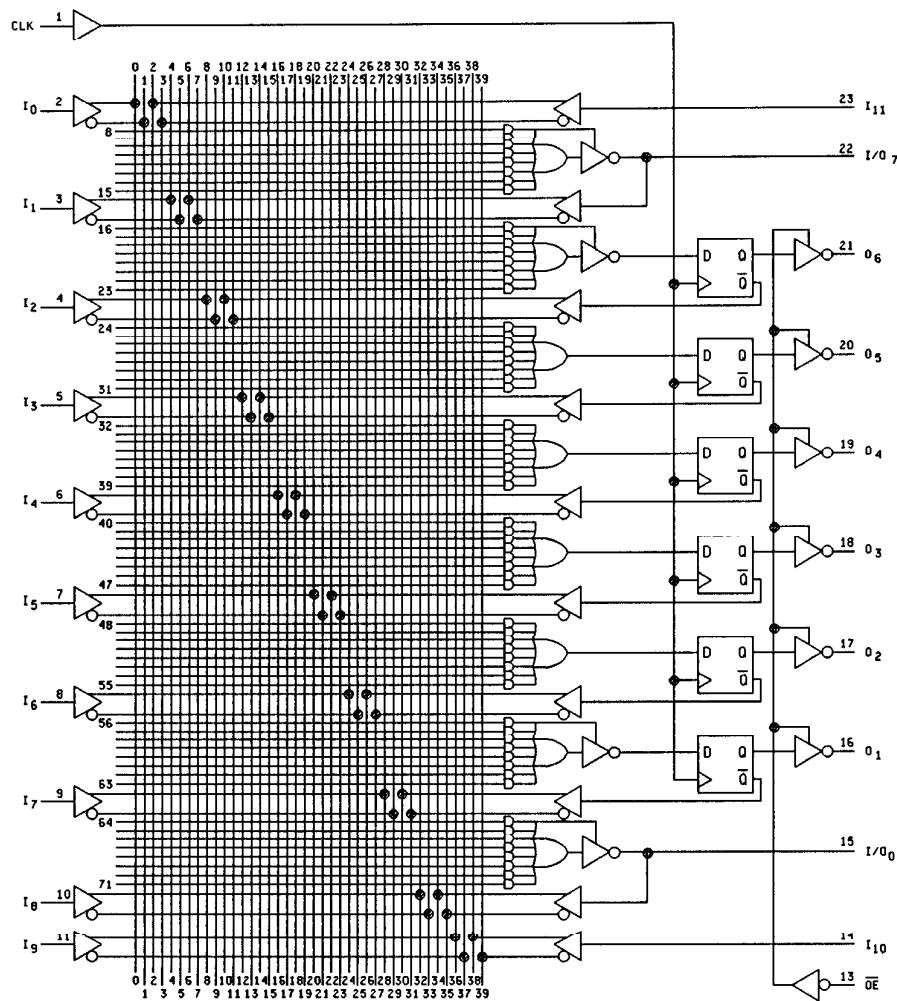
Device type 04

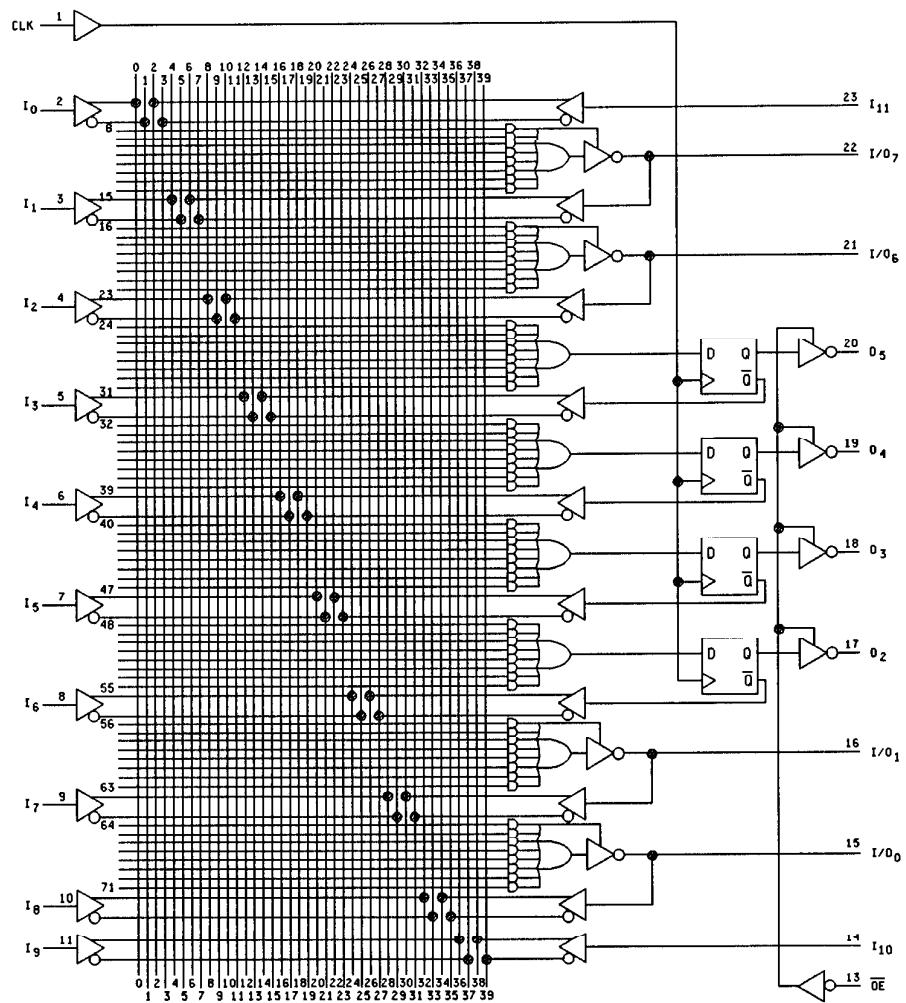
INPUTS															OUTPUTS							
\overline{OE}	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0	CLK	I/07	I/06	05	04	03	02	I/01	I/00	
H	X	X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	7	Z	
L	X	X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	H	H	H	H	Z	Z	

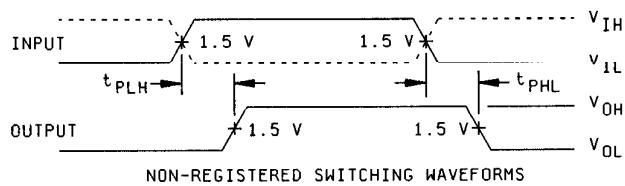
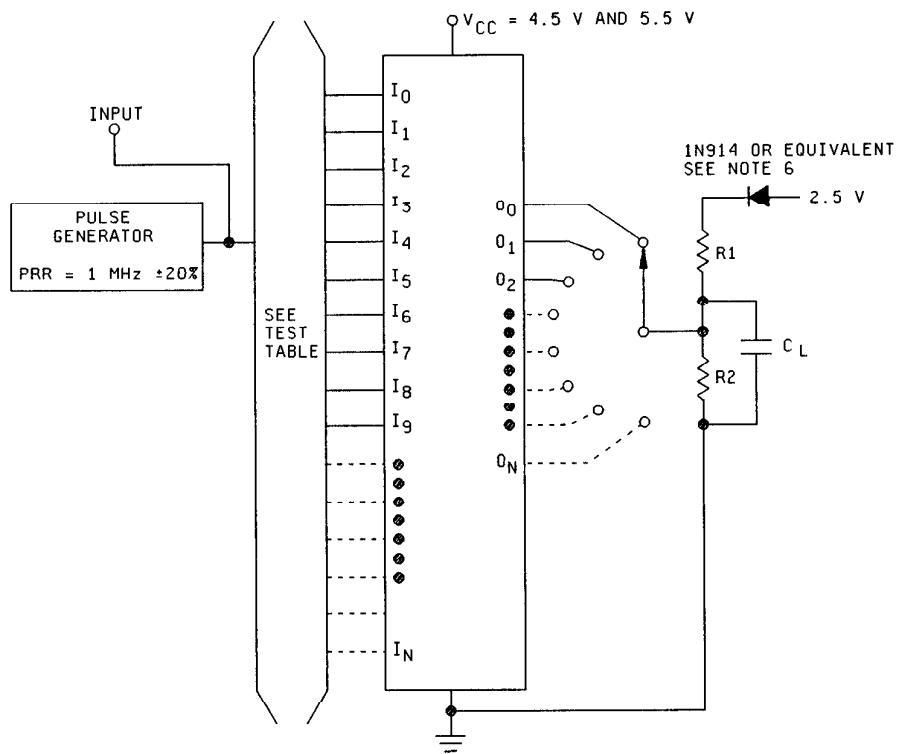
FIGURE 2. Truth tables (unprogrammed).

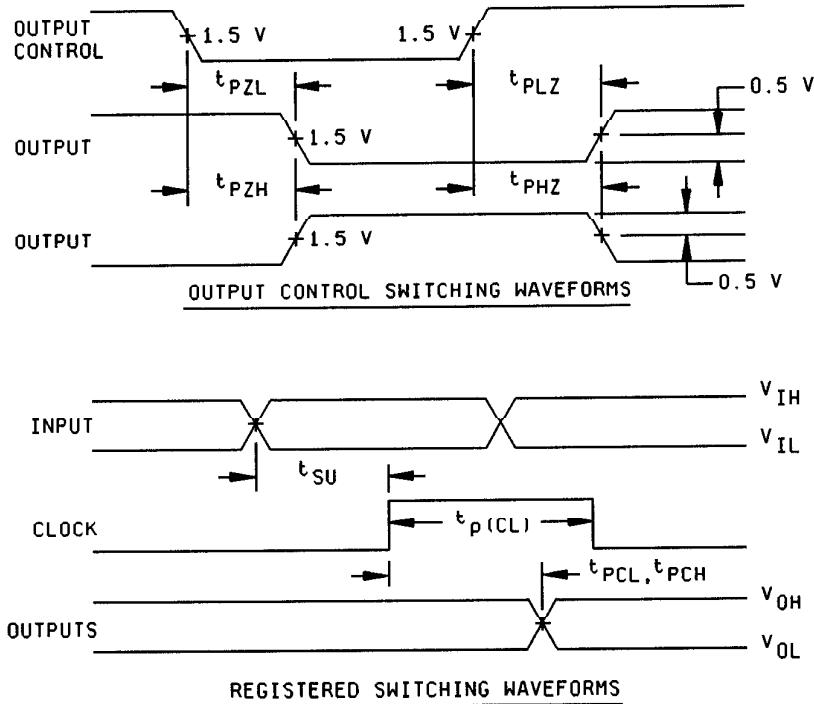
Device type 01FIGURE 3. Unprogrammed logic diagram.

Device type 02FIGURE 3. Unprogrammed logic diagram - continued.

FIGURE 3. Unprogrammed logic diagram - Continued.

Device type 04FIGURE 3. Unprogrammed logic diagram - Continued.

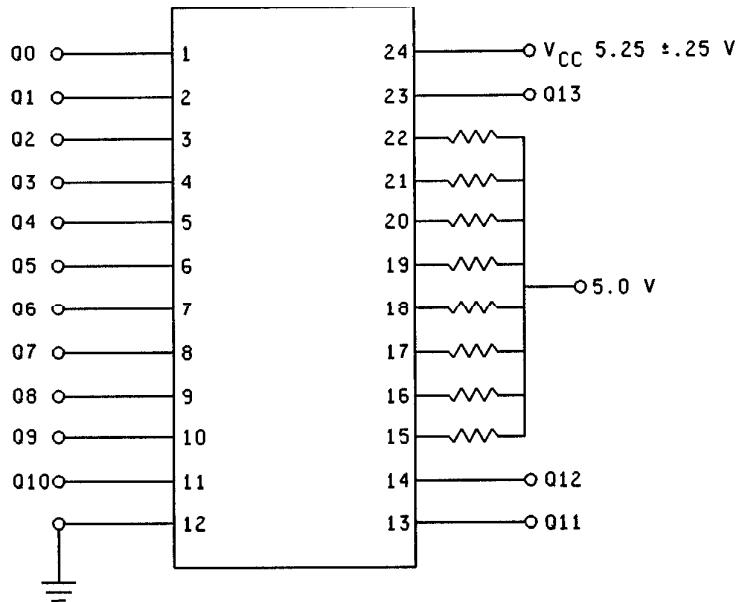
FIGURE 4. Switching time test circuit and waveforms.



NOTES:

1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting device.
2. $C_L = 45 \text{ pF}$ minimum, including jig and probe capacitance; $R1 = 200\Omega \pm 2\%$; $R2 = 390\Omega \pm 2\%$.
3. Outputs may be under load simultaneously.
4. Requirements for $t_p(C_L)$, t_{SU} , and t_H are established by setting parameters to the limits in table I and observing proper output state changes.
5. $V_{IH} = 3.0 \text{ V}$; $V_{IL} = 0.0 \text{ V}$.
6. For circuit C, the diode/VBIAS = 2.5 V may be replaced with switch S1, and VBIAS of 5.0 V. S1 is open for t_{PZH} , t_{PHZ} , and Fmax tests.

FIGURE 4. Switching time test circuit and waveforms - Continued.



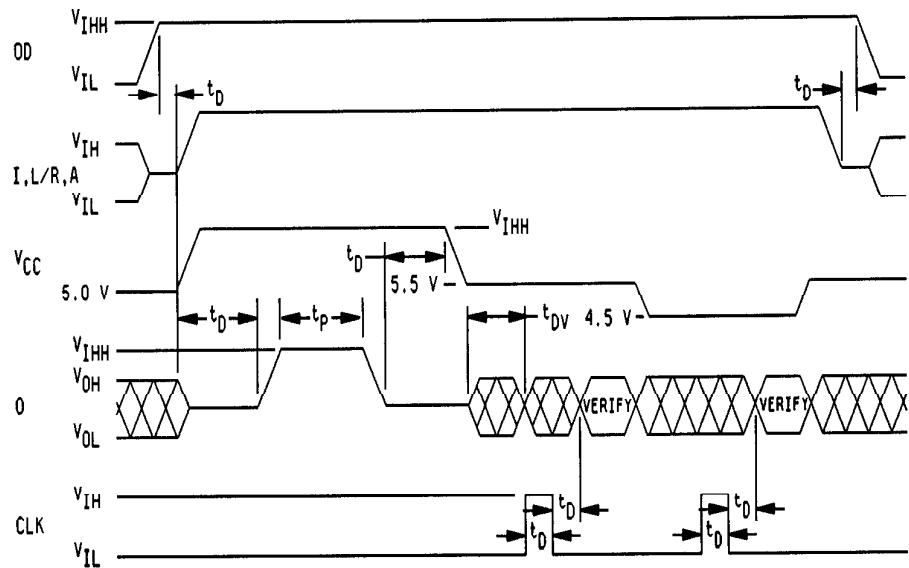
NOTES:

1. $R = 33\Omega \pm 5\%$. All outputs shall have separate identical loads.
2. All pulse generators have the following characteristics:
 $V_{IL} = 1.5$ V minimum to 0.8 V maximum; $V_{IH} = 2.0$ V minimum to 5.5 V maximum;
 50% ±15% duty cycle and frequencies as specified in note 3.
3. Input frequencies are as follows:

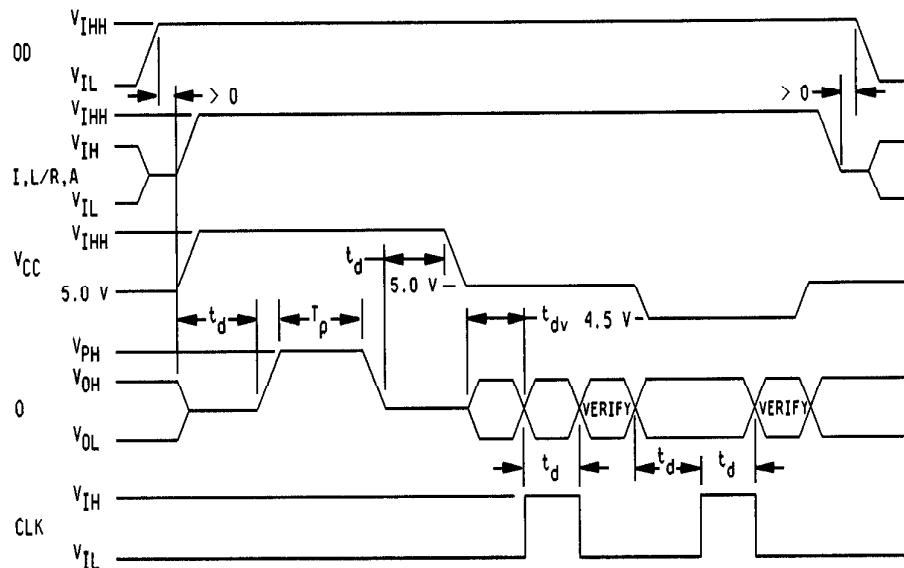
<u>Input</u>	<u>Frequency ($\pm 50\%$)</u>	<u>Input</u>	<u>Frequency ($\pm 50\%$)</u>
Q0	$f_0 = 100$ kHz	Q7	$f_7 = 1/128 f_0$
Q1	$f_1 = 1/2 f_0$	Q8	$f_8 = 1/256 f_0$
Q2	$f_2 = 1/4 f_0$	Q9	$f_9 = 1/512 f_0$
Q3	$f_3 = 1/8 f_0$	Q10	$f_{10} = 1/1024 f_0$
Q4	$f_4 = 1/16 f_0$	Q11	$f_{11} = 1/2048 f_0$
Q5	$f_5 = 1/32 f_0$	Q12	$f_{12} = 1/4096 f_0$
Q6	$f_6 = 1/64 f_0$	Q13	$f_{13} = 1/8192 f_0$

FIGURE 5. Burn-in and life test circuit.

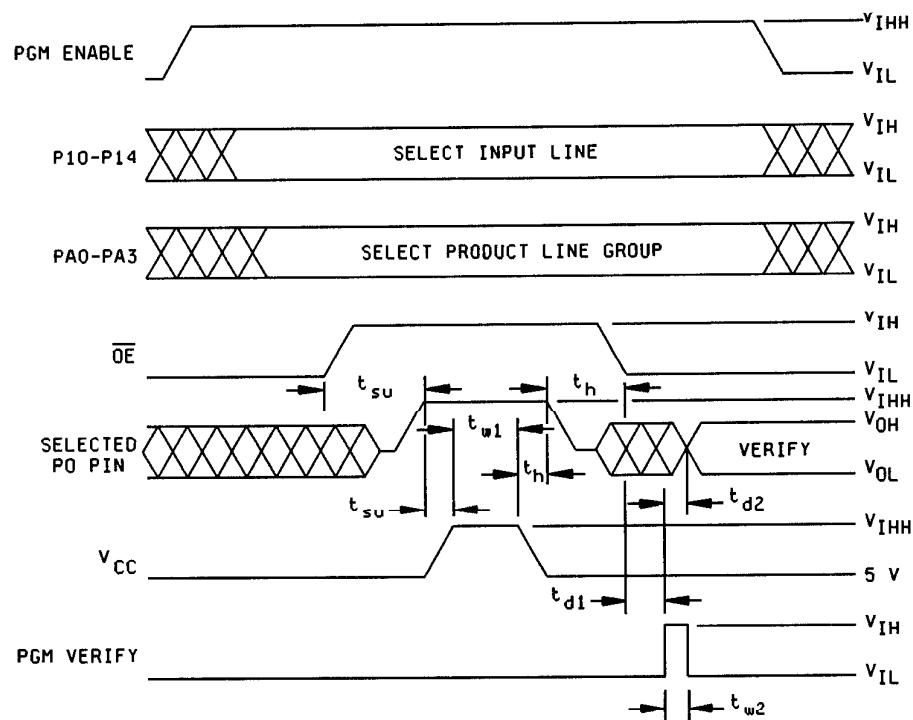
Circuit A



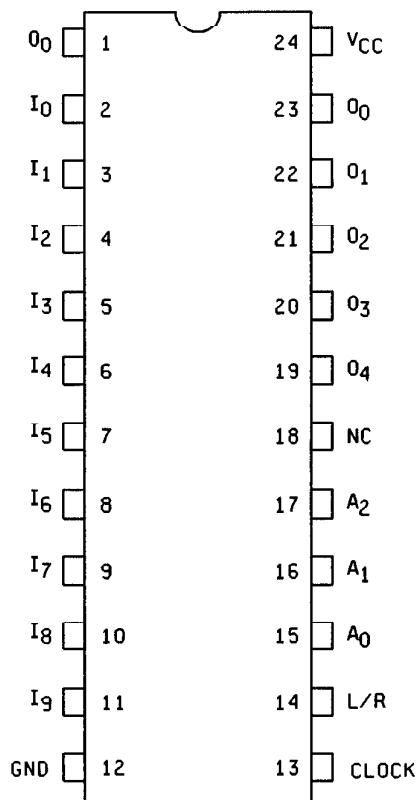
Circuit B

FIGURE 6. Programming waveforms.

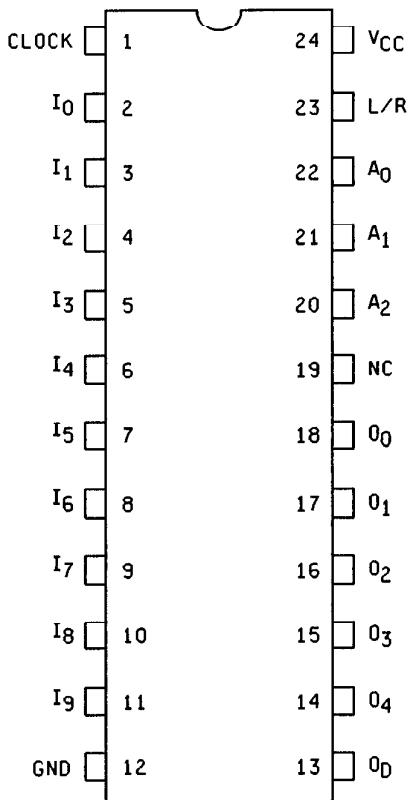
Circuit C

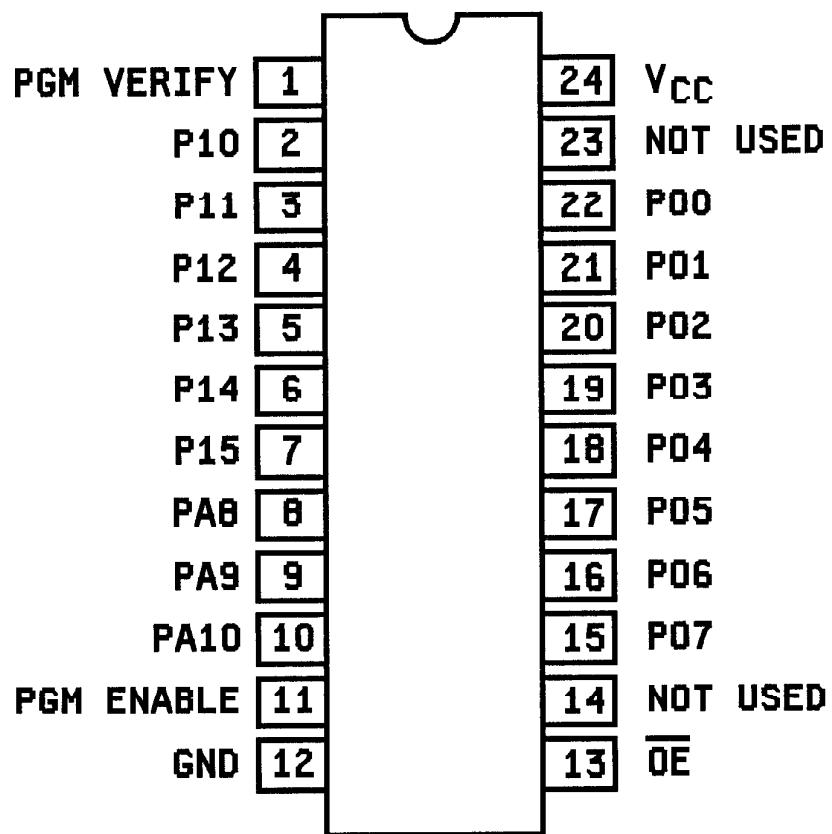
FIGURE 6. Programming waveforms - Continued.

PRODUCTS 0 THRU 39



PRODUCTS 40 THRU 79

FIGURE 7. Programming pin identification for circuit A and circuit B.

FIGURE 7. Programming pin identification for circuit C - Continued.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady state life test (method 1005 of MIL-STD-883) conditions:
 - (1) Test condition D, using the circuit shown on figure 4, or equivalent.
 - (2) $T_A = +125^\circ\text{C}$ minimum.
 - (3) Test duration: 1,000 hours except, as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.
- c. For qualification, at least 50 percent of the sample selected for testing in subgroup 1 shall be programmed (see 5.2.2). For quality conformance inspection, the programmability sample (sec 4.4.1e) shall be included in the subgroup 1 tests.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows:

End-point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Programming/verifying procedure for circuit A, B, and C. Use the programming specifications on figure 6a, figure 7a, and table III for circuit A; use figure 6b, figure 7a, and table VI for circuit B; use figure 6c, figure 7b, and table IX for circuit C; and the following procedures shall be used for programming the device.

4.6.1 Preverification.

4.6.1.1 Circuits A and B.

- a. Raise V_{CC} to 5.0 volts.
- b. Raise output disable pin, OD, to V_{IHH} .
- c. Select an input line by specifying inputs and L/R as shown in table IV for circuit A, and table VII for circuit B.
- d. Select a product line by specifying A0, A1, and A2 one-of-eight select as shown in table V for circuit A, and table VIII for circuit B.
- e. Pulse the clock pin and verify (with clock at V_{IL}) that the output pins, 00 through 03, are in the state corresponding to an unblown fuse. Use the minimum timing conditions as specified on figure 6a for circuit A, and figure 6b for circuit B.
 - (1) For verified unblown condition, continue procedure from 4.6.1.1c through 4.6.1.1e.
 - (2) For verified blown condition, stop procedure.

4.6.1.2 Circuit C.

- a. Raise V_{CC} to 5.0 V.
- b. Raise PGM ENABLE pin to V_{IHH} .
- c. Select an Input line by applying appropriate logic levels to PI pins.
- d. Select a Product line by applying appropriate logic levels to PA pins.
- e. Pulse PGM VERIFY pin to V_{IH} using the minimum timing conditions specified in Table IX, and verify that the outputs 00-07 are in the state corresponding to an unblown fuse.
 - (1) For verified unblown condition, continue procedure from 4.6.1.1c to 4.6.1.1e.
 - (2) For verified blown condition stop procedure.

TABLE III. Programming characteristics for circuit A.

Symbol	Parameters	Limits			Unit
		Min	Typ	Max	
V_{IHH}	Program-level input voltage	11.5	11.75	12.0	V
I_{IHH}	Program-level input current	50			
	Output program pulse output disable, OD		50		mA
	All other inputs		10		
I_{CCH}	Program supply current			900	mA
T_p	Program pulse width	10	20	50	μs
t_d	Delay time	100			ns
	Program pulse duty cycle			20	μ
V_p	Program/verify - protect input voltage	18	18.5	19	V
I_p	Program verify - protect input current			400	mA
T_{PP}	Security fuse programming pulse width	10	40	70	μs
	Security fuse programming duty cycle			50	%
t_{RP}	Rise time of output programming and address pulses	1	1.5	10	V/ μs
t_{RP}	Rise time of security use programming pulses	1	1.5	10	V/ μs
V_{CCPP}	V_{CC} value during security fuse programming	5.75	6.0	6.25	V
	V_{CC} value for first verify	4.75	5.0	5.25	
	V_{CC} value for high V_{CC} verify	5.4	5.5	5.6	
	V_{CC} value for low V_{CC} verify	4.4	4.5	4.6	

TABLE IV. Input Line select for circuit A.

Input Line number	Pin identification											L/R
	I ₉	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	L/R	
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	Z	
1	HH	HH	HH	HH	HH	HH	HH	HH	HH	II	Z	
2	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	
3	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	
4	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	Z	
5	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	Z	
6	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	
7	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	
8	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	Z	
9	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	Z	
10	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	III
11	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	
12	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	Z	
13	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	
14	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	
15	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	
16	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	Z	
17	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	
18	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	
19	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	
20	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	Z	
21	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	
22	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	
23	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	
24	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	Z	
25	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	
26	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	
27	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	
28	HH	HH	L	HH	Z							
29	HH	HH	H	HH	Z							
30	HH	HH	L	HH	HH							
31	HH	HH	H	HH	HH							
32	HH	L	HH	Z								
33	HH	H	HH	Z								
34	H	L	HH	HH								
35	HH	H	HH	HH								
36	L	HH	Z									
37	H	HH	Z									
38	L	HH	HH									
39	H	HH	HH									

Voltage legend:

L = Low level input voltage (V_{IL}).H = High level input voltage (V_{IH}).HH = High level program voltage (V_{IHH}).

Z = High impedance (e.g., 10 kΩ to 5.0 V).

TABLE V. Product line select for circuit A.

Product line number	Pin identification							
	O_4	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0, 40	Z	Z	Z	Z	HH	Z	Z	Z
1, 41	Z	Z	Z	Z	HH	Z	Z	HH
2, 42	Z	Z	Z	Z	HH	Z	HH	Z
3, 43	Z	Z	Z	Z	HH	Z	HH	HH
4, 44	Z	Z	Z	Z	HH	HH	Z	Z
5, 45	Z	Z	Z	Z	HH	HH	Z	HH
6, 46	Z	Z	Z	Z	7	HH	HH	Z
7, 47	Z	Z	Z	Z	HH	HH	HH	HH
8, 48	Z	Z	Z	HH	Z	Z	Z	Z
9, 49	Z	Z	Z	HH	Z	Z	Z	HH
10, 50	Z	Z	Z	HH	Z	Z	HH	Z
11, 51	Z	Z	Z	HH	Z	Z	HH	HH
12, 52	Z	Z	Z	HH	Z	HH	Z	Z
13, 53	Z	Z	Z	HH	Z	HH	Z	HH
14, 54	Z	Z	Z	HH	Z	HH	HH	Z
15, 55	Z	Z	Z	HH	Z	HH	HH	HH
16, 56	Z	Z	HH	Z	Z	Z	Z	Z
17, 57	Z	Z	HH	Z	Z	Z	Z	HH
18, 58	Z	Z	HH	Z	Z	Z	Z	HH
19, 59	Z	Z	HH	Z	Z	Z	HH	HH
20, 60	Z	Z	HH	Z	Z	HH	Z	Z
21, 61	Z	Z	HH	Z	Z	HH	Z	HH
22, 62	Z	Z	HH	Z	Z	HH	HH	Z
23, 63	Z	Z	HH	Z	Z	HH	HH	HH
24, 64	Z	HH	Z	Z	Z	Z	Z	Z
25, 65	Z	HH	Z	Z	Z	Z	Z	HH
26, 66	Z	HH	Z	Z	Z	Z	HH	Z
27, 67	Z	HH	Z	Z	Z	Z	Z	HH
28, 68	Z	HH	Z	Z	Z	HH	Z	Z
29, 69	Z	HH	Z	Z	Z	HH	Z	HH
30, 70	Z	HH	Z	Z	Z	HH	HH	Z
31, 71	Z	HH	Z	Z	Z	HH	HH	HH
32, 72	HH	Z	Z	Z	Z	Z	Z	Z
33, 73	HH	Z	Z	Z	Z	Z	Z	HH
34, 74	HH	Z	Z	Z	Z	Z	HH	Z
35, 75	HH	Z	Z	Z	Z	Z	HH	HH
36, 76	HH	Z	Z	Z	Z	HH	Z	Z
37, 77	HH	Z	Z	Z	Z	HH	Z	HH
38, 78	HH	Z	Z	Z	Z	HH	HH	Z
39, 79	HH	Z	Z	Z	Z	HH	HH	HH

Voltage legend;

HH = High level program voltage (V_{IHH}).Z = High impedance (e.g., 10 k Ω to 5.0 v).

TABLE VI. Programming characteristics for circuit B.

Symbol	Parameter	Limits			Units
		Min	Typ	Max	
V_{THH}	Program-level input voltage	11.0	11.5	12.0	V
I_{IHH}	Output program pulse			50	
	Program level input current OE, L/R			25	mA
	All other inputs			5	
I_{CCH}	Program supply current			400	mA
T_p	Program pulse width	10		50	μs
t_d	Delay time	100			ns
---	Program pulse duty cycle			25	%
V_p	Program verify protect-input voltage		20		V
I_p	Program verify protect-input current			400	mA
t_{dv}	Delay time to verify	100			μs
V_{PH}	Programming pulse	11.0	11.5	12.0	V

TABLE VII. Input Line select for circuit B.

Input Line number	Pin identification											
	I ₉	I ₈	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	L/R	
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	Z	
1	HH	HH	HH	HH	HH	HH	HH	HH	H	Z		
2	HH	HH	HH	HH	HH	HH	HH	HH	L	HH		
3	HH	HH	HH	HH	HH	HH	HH	HH	H	HH		
4	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	Z	
5	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	Z	
6	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	
7	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	
8	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	Z	
9	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	Z	
10	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	
11	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	
12	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	Z	
13	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	Z	
14	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	
15	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	
16	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	Z	
17	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	Z	
18	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	
19	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	
20	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	Z	
21	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	Z	
22	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	
23	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	
24	HH	HH	L	HH	Z							
25	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	Z	
26	HH	HH	L	HH	HH							
27	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	
28	HH	HH	L	HH	Z							
29	HH	HH	H	HH	Z							
30	HH	HH	L	HH	HH							
31	HH	HH	H	HH	HH							
32	HH	L	HH	Z								
33	HH	H	HH	Z								
34	HH	L	HH	HH								
35	HH	H	HH	HH								
36	L	HH	Z									
37	H	HH	Z									
38	L	HH	HH									
39	H	HH	HH									

Voltage legend:

L = Low level input voltage (V_{IL}).H = High level input voltage (V_{IH}).HH = High level program voltage (V_{IHH}).

Z = High impedance (e.g., 10 kΩ to 5.0 V)

TABLE VIII. Product line select for circuit B.

Product line number	Pin identification							
	O_4	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0, 40	Z	Z	Z	Z	HH	Z	Z	Z
1, 41	Z	Z	Z	Z	HH	Z	Z	HH
2, 42	Z	Z	Z	Z	HH	Z	HH	Z
3, 43	Z	Z	Z	Z	HH	Z	HH	HH
4, 44	Z	Z	Z	Z	HH	HH	Z	Z
5, 45	Z	Z	Z	Z	HH	HH	Z	HH
6, 46	Z	Z	Z	Z	HH	HH	HH	Z
7, 47	Z	Z	Z	Z	HH	HH	HH	HH
8, 48	Z	Z	Z	HH	7	7	Z	Z
9, 49	Z	Z	Z	HH	Z	Z	Z	HH
10, 50	Z	Z	Z	HH	Z	Z	HH	Z
11, 51	Z	Z	Z	HH	Z	Z	HH	HH
12, 52	Z	Z	Z	HH	Z	HH	Z	Z
13, 53	Z	Z	Z	HH	Z	HH	Z	HH
14, 54	Z	Z	Z	HH	Z	HH	HH	Z
15, 55	Z	Z	Z	HH	Z	HH	HH	HH
16, 56	Z	Z	HH	Z	Z	Z	Z	Z
17, 57	Z	Z	HH	Z	Z	Z	7	HH
18, 58	Z	Z	HH	Z	Z	Z	HH	Z
19, 59	Z	Z	HH	Z	Z	Z	HH	HH
20, 60	Z	Z	HH	Z	Z	HH	Z	Z
21, 61	Z	Z	HH	Z	Z	HH	Z	HH
22, 62	Z	Z	HH	Z	Z	HH	HH	Z
23, 63	Z	Z	HH	Z	Z	HH	HH	HH
24, 64	Z	HH	Z	Z	Z	Z	Z	Z
25, 65	Z	HH	Z	Z	Z	Z	Z	HH
26, 66	Z	HH	Z	Z	Z	Z	HH	Z
27, 67	Z	HH	Z	Z	Z	Z	HH	HH
28, 68	Z	HH	Z	Z	Z	HH	Z	Z
29, 69	Z	HH	Z	Z	Z	HH	Z	HH
30, 70	Z	HH	Z	Z	Z	HH	HH	Z
31, 71	Z	HH	Z	Z	Z	HH	HH	HH
32, 72	HH	Z	Z	Z	Z	Z	Z	Z
33, 73	HH	Z	Z	Z	Z	Z	Z	HH
34, 74	HH	Z	Z	Z	Z	Z	HH	Z
35, 75	HH	Z	Z	Z	Z	Z	HH	HH
36, 76	HH	Z	Z	Z	Z	HH	Z	Z
37, 77	HH	Z	Z	Z	Z	HH	Z	HH
38, 78	HH	Z	Z	Z	Z	HH	HH	Z
39, 79	HH	Z	Z	Z	Z	HH	HH	HH

Voltage legend:

HH = High level program voltage, V_{IHH} .

Z = High impedance (e.g., 10 kΩ to 5.0 V)

Table IX. Programming characteristics for circuit C.

Symbol	Description	Min	Nom	Max	Unit
V_{CC}	Verify level supply voltage	5.25	5.50	5.75	V
V_{IH}	High level input voltage	2.40		5.50	V
V_{IL}	Low level input voltage			.50	V
V_{IHH}	Program pulse voltage	10.25	10.50	10.75	V
I_{IHH}	Program pulse current	PO PGM, ENA, OE PI, PA I_{CC}	20 10 10 500	50 25 25 50	mA
t_{w1}	Program pulse duration at PO	10		50	μs
t_{su}	Set up time	100			ns
t_h	Hold time	100			ns
t_{d1}	Delay time from OE low to PGM verify	100			ns
t_{d2}	Delay time from PGM verify to valid output	200			ns
t_{w2}	Pulse duration at PGM verify	100			ns

Table X. Input line select for circuit C.

INPUT LINE NUMBER	Input Line number address pin states						
	PIO	PI1	PI2	PI3	PI4	PI5	HEX
00	L	L	L	L	L	L	00
01	L	L	L	L	L	H	01
02	L	L	L	L	H	L	02
03	L	L	L	L	H	H	03
04	L	L	L	H	L	L	04
05	L	L	L	H	L	H	05
06	L	L	L	H	H	L	06
07	L	L	L	H	H	H	07
08	L	L	H	L	L	L	08
09	L	L	H	L	L	H	09
10	L	L	H	L	H	L	0A
11	L	L	H	L	H	H	0B
12	L	L	H	H	L	L	0C
13	L	L	H	H	L	H	0D
14	L	L	H	H	H	L	0E
15	L	L	H	H	H	H	0F
16	L	H	L	L	L	L	10
17	L	H	L	L	L	H	11
18	L	H	L	L	H	L	12
19	L	H	L	L	H	H	13
20	L	H	L	H	L	L	14
21	L	H	L	H	L	H	15
22	L	H	L	H	H	L	16
23	L	H	L	H	H	H	17
24	L	H	H	L	L	H	18
25	L	H	H	L	L	H	19
26	L	H	H	L	H	L	1A
27	L	H	H	L	H	H	1B
28	L	H	H	H	L	L	1C
29	L	H	H	H	L	H	1D
30	L	H	H	H	H	L	1E
31	L	H	H	H	H	H	1F
32	H	L	L	L	L	L	20
33	H	L	L	L	L	H	21
34	H	L	L	L	L	L	22
35	H	L	L	L	H	H	23
36	H	L	L	H	L	L	24
37	H	L	L	H	L	H	25
38	H	L	L	H	H	L	26
39	H	L	L	H	H	H	27
SF	H	H	H	H	H	H	3F

Table XI. Product term addressing for circuit C.

PRODUCT TERMS								ADDRESS PIN STATES		
P00	P01	P02	P03	P04	P05	P06	P07	PA8	PA9	PA10
00	08	16	24	32	40	48	56	L	L	L
01	09	17	25	33	41	49	57	L	L	H
02	10	18	26	34	42	50	58	L	H	L
03	11	19	27	35	43	51	59	L	H	H
04	12	20	28	36	44	52	60	H	L	L
05	13	21	29	37	45	53	61	H	L	H
06	14	22	30	38	46	54	62	H	H	L
07	15	23	31	39	47	55	63	H	H	H
--	--	--	--	--	--	--	--	X	X	H

SF - Security fuse (does not require voltage to the P0 pin).

4.6.2 Programming algorithm.

4.6.2.1 Circuits A and B.

- a. Rise output disable pin, OE, to V_{IHH} .
- b. Lower clock pin to V_{IL} .
- c. Select an input line as specified in 4.6.1.1c.
- d. Select a product line as specified in 4.6.1.1d.
- e. Raise V_{CC} to V_{IHH} .
- f. Program the fuse by pulsing the output pins of the selected group (one at a time) to V_{IHH} (see figure 6a for circuit A, and figure 6b for circuit B).
- g. Lower V_{CC} to 5.0 volts.
- i. Repeat this procedure from 4.6.2.1c until pattern is complete.

4.6.2.2 Circuit C.

- a. Raise PGM ENABLE pin to V_{IHH} .
- b. Select an input line as in 4.6.1.2c.
- c. Select a product line as in 4.6.1.2d.
- d. Raise \overline{OE} to V_{IH} .
- e. Raise selected PO pin to V_{IHH} .
- f. Program the fuse by pulsing V_{CC} to V_{IHH} .
- g. Remove output voltage.
- h. Repeat this procedure from 4.6.2.2b until entire pattern is complete.

4.6.3 First verification pass for all fuse locations.

4.6.3.1 Circuits A and B.

- a. Raise V_{CC} to 4.5 volts.
- b. Select input line as specified in 4.6.1.1c.
- c. Select a product line as specified in 4.6.1.1d.

- d. Pulse the clock pin and verify (with clock at V_{IL}) that the output pins, 00 through 03 are in the correct state.
 - (1) For verified output state, continue procedure.
 - (2) For overblown conditions, stop procedure.
 - (3) For underblown condition, reject part
- e. Repeat this procedure from 4.6.3.1b until the entire array is exercised.

4.6.3.2 Circuit C.

- a. Raise V_{CC} to 4.5 V.
- b. Raise PGM ENABLE pin to $V_{I(HI)}$.
- c. Select an input line as specified in 4.6.1.2c.
- d. Select a product line as specified in 4.6.1.2d.
- e. Pulse PGM VERIFY pin and verify that the outputs 00-07 are in the correct state.
 - (1) For verified output condition continue the procedure.
 - (2) For overblown condition, stop procedure.
 - (3) For underblown condition, reject the part.
- f. Repeat this procedure from 4.6.3.1c until the entire array is exercised.

4.6.4 High voltage verify for all fuse locations.

4.6.4.1 Circuits A and B.

- a. Raise V_{CC} to 5.5 volts.
- b. Repeat from 4.6.3.1b to 4.6.3.1d until the entire array is exercised.

Programming should be attempted at room temperature, 15°C to 30°C. To prevent further programming, security fuses may be blown. Raise V_{CC} to 6.0 volts, and raise pins 1 and 11 to V_p for 10 milliseconds to 1 second.

4.6.4.2 Circuit C.

- a. Raise V_{CC} to 5.5 V
- b. Repeat procedure from 4.6.3.2c until the entire array is exercised.

Security fuse information: The security fuse is programmed using procedure in 4.6.2.2 omitting steps 4.6.2.2e and 4.6.2.2h.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.2 Ordering data. Acquisition documents should specify the following:

- a. Complete PIN (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.

- f. Requirements for product assurance options.
- g. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the PIN. Unless otherwise specified, these requirements will not apply to direct purchase by, or direct shipment to the Government.
- h. Requirement for programming the device, including processing option.
- i. Requirement for "JAN" marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, and as follows:

GND - - - - - Ground zero voltage potential.
 V_{IN} - - - - - Voltage level at an input terminal.
 V_{IC} - - - - - Input clamp voltage.
 I_{IN} - - - - - Current flowing into an input terminal.

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number. It is intended that spare devices for logistic support be acquired in the unprogrammed condition (see 3.7.1) and programmed by the maintenance activity, except where use of quantities for devices with a specific program or pattern justify stocking of preprogrammed devices.

6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed Generic-Industry type. Generic-Industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-35810 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of Generic-Industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type/manufacturer	Circuit designator	Fusible link	Symbol FSCM number
01	PAL20L8A/Monolithic Memories	A	Tiw	CECD/50364
01	PAL20L8A/National	B	Tiw	CCXP/27014
01	PAL20L8A/Texas Instruments	C	Tiw	CGO/01295
02	PAL20R8A/Monolithic Memories	A	Tiw	---
02	PAL20R8A/National	B	Tiw	---
02	PAL20R8A/Texas Instruments	C	Tiw	---
03	PAL20R6A/Monolithic Memories	A	Tiw	---
03	PAL20R6A/National	B	Tiw	---
03	PAL20R6A/Texas Instruments	C	Tiw	---
04	PAL20R4A/Monolithic Memories	A	Tiw	---
04	PAL20R4A/National	B	Tiw	---
04	PAL20R4A/Texas Instruments	C	Tiw	---

6.6 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

CONCLUDING MATERIAL

Custodian:
 Army - ER
 Navy - EC
 Air Force - 17

Preparing activity:
 Air Force - 17

Review activities:
 Air Force - 19, 85, 99
 DLA - ES

(Project 5962-1285)

Agent:
 DLA - ES